What is claimed is:

1. A method of forming a semiconductor device comprising:

a) forming a gate structure over a substrate being doped with a first conductivity type impurity;

b) performing a doped depletion region implantation by implanting ions being the second conductive type to the substrate to form doped depletion regions beneath and separated from said source/drain regions;

c) performing a S/D implant by implanting ions having a second conductivity type into the substrate to form S/D regions adjacent to said gate;

(1) said doped depletion regions have an impurity concentration and thickness so that said doped depletion regions are depleted due to a built-in potential created between said doped depletion regions and said substrate.

2. The method of claim 1 wherein doped depletion region are not formed under said gate structure.

3. The method of claim 1 which further includes said doped depletion regions have a impurity concentration so that the built-in junction potential between said doped depletion regions and said substrate forms depletion regions in the substrate between the source/drain regions and the doped depletion region;

said depletion regions have a net impurity concentration of the first conductivity type.

4. The method of claim 1 which further includes said doped depletion regions have a impurity concentration so that the built-in junction potential between said doped depletion regions and said substrate forms depletion regions in the substrate between the source/drain regions and the doped depletion region; said depletion regions have a net impurity concentration of the first conductivity type;

said depletion regions have a net impurity concentration between 1E16 to 5E18 atom/cc.

5. The method of claim 1 which further includes implanting ions of a first impurity type into said substrate between said source/drain regions and said doped depletion regions.

6. The method of claim 1 which further includes performing an implant type selected from the group consisting of Halo implant, threshold voltage implant, and a field implant, that implant ions of a first impurity type into said substrate at least between said source/drain regions and said doped depletion regions.

7. The method of claim 1 wherein the region of said substrate between said source/drain regions and said doped depletion regions has a concentration of a first type impurity between 1E16 to 1E18 atom/cc;

a channel region in said substrate under said gate structure; said channel region has a concentration of a second type impurity between 1E16 to 1E18 atom/cc.

8. The method of claim 1 wherein said depletion regions are fully depleted.

9. The method of claim 1 which further includes performing LDD implantation by implanting ions being a second type into the substrate using the gate structure as a mask to form LDD regions.

10. The method of claim 1 which further includes performing LDD implantation by implanting ions being a second type into the substrate using the gate structure as a mask to form LDD regions;

the LDD regions are formed before the doped depletion regions.

11. The method of claim 1 which further includes performing LDD implantation by implanting ions being a second type into the substrate using the gate structure as a mask to form LDD regions;

wherein the doped depletion regions are formed after the LDD regions.

12. The method of claim 1 wherein said first conductive type is p-type and said substrate has a boron concentration between 1E17 to 1E19 atom/cc.

13. The method of claim 1 wherein said first conductive type is n-type and said substrate 100 has a As or P concentration between 1E 17 to 1E 19 atom/cc.

14. The method of claim 1 wherein said first conductive type substrate is comprised of Si or SiGe or strained Si, or relaxed SiGe or strained Ge.

15. The method of claim 1 wherein said gate structure has a channel width between 0.04 and 0.5 μm.

16. The method of claim 1 wherein the LDD implantation is performed by implanting As ions at a dose between 5E14 and 1E16 atoms /cm^2, at an energy between 1keV and 10 keV.

17. The method of claim 1 wherein the LDD implantation is performed by implanting Boron ions at a dose between 1E14 and 5E15 atoms /cm^2, at an energy between 1 keV and 10 keV.

18. The method of claim 1 wherein the doped depletion region implantation is performed by implanting As or P ions at a does between 5E12 and 5E13 atoms/cm2, at an energy between 100 keV and 500 keV; said doped depletion region has a minimum depth below the substrate surface between 0.09 and 0.7 μm.

19. The method of claim 1 wherein the doped depletion region implantation is performed by implanting boron ions at a does between 5E11 and 5E13 atoms/cm2, at an energy between 50 keV and 200 keV; said doped depletion region has a minimum depth below the substrate surface between 0.09 and 0.7 μm.

20. The method of claim 1 wherein the S/D implant is performed by implanting arsenic (As) or phosphorus (P) ions at a dose between 5E14 to 1E16 atoms/cm2, at an energy between 50 keV and 80 keV; said Source/drain regions have a depth below the substrate surface of between 0.04 and 0.5 μm.

21. The method of claim 1 wherein said second conductivity type is p-type; and said S/D implant is performed by implanting boron ions at a dose between 5E14 to 1E16 atoms/cm^2, at an energy between 50keV and 80keV; said source/drain regions have a depth below the substrate surface of between 0.04 and 0.5 μm.

22. The method of claim 1 which further includes forming one or more spacers on the sidewalls of said gate structure.

23. A method of forming a semiconductor device comprising:

a) forming a gate structure over on substrate being doped with a first conductivity type impurity;

b) performing a doped depletion region implantation by implanting ions being the second conductive type to the substrate to form doped depletion regions beneath and separated from said source/drain regions;

(1) said doped depletion regions have an impurity concentration and thickness so that said doped depletion regions are depleted due to a built-in potential created between said doped depletion regions and said substrate;

(2) said doped depletion regions have a impurity concentration so that the built-in junction potential between said doped depletion regions and said substrate forms depletion regions in the substrate between the source/drain regions and the doped depletion region; said depletion regions have a net impurity concentration of the first conductivity type; said depletion regions have a net impurity concentration between 1E16 to 1E18 atom/cc;

c) performing a S/D implant by implanting ions having a second conductivity type into the substrate to form S/D regions adjacent to said gate;

(1) said substrate between said source/drain regions and said doped depletion regions has a concentration of a first type impurity between 1E16 to 1E18 atom/cc.

24. The method of claim 23 wherein doped depletion region are not formed under said gate structure.

25. The method of claim 23 wherein the region of said substrate between said source/drain regions and said doped depletion regions has a concentration of a first type impurity between 1E16 to 1E18 atom/cc;
a channel region in said substrate under said gate structure; said channel region has a concentration of a second type impurity between 1E16 to 1E18 atom/cc.

26. The method of claim 23 which further includes forming one or more spacers on the sidewalls of said gate structure.

27. The method of claim 23 which further includes forming two or more spacers on the sidewalls of said gate structure prior to the doped depletion region implantation.

28. A semiconductor device comprising:

a semiconductor substrate having a surface; said semiconductor substrate being doped with a first conductivity type impurity; the top portion of said semiconductor substrate is comprised of a first doped layer of a first conductivity type;

a gate structure over the surface of said semiconductor substrate; said gate structure comprising a gate dielectric layer and a gate electrode;

source/drain regions in said semiconductor substrate to oppose each other with a channel region laterally residing therebetween at a location immediately beneath said gate structure,

doped depletion regions of a second conductivity type in said a first doped layer of a first conductivity type under said source/drain regions;

doped depletion regions are determined in impurity concentration and thickness to ensure that this layer is fully depleted due to a built-in potential creatable between said substrate and doped depletion regions;

whereby said doped depletion regions reduce the capacitance between the source/drain regions and the substrate.

29. The semiconductor device of claim 28 which further includes said doped depletion regions under said source/drain regions, but not under said channel region.

30. The semiconductor device of claim 28 which further includes LDD regions that extend from said source/drain regions toward said channel region; said LDD regions being lower in impurity concentration and shallower in depth than said source/drain region.

31. The semiconductor device of claim 28 which further includes depletion regions and S/D depletion regions adjacent said doped depletion regions and between said source/drain regions: and

said doped depletion regions and; said depletion regions have a net impurity concentration of the first conductivity type.

32. The semiconductor device of claim 28 which further includes depletion regions between said source/drain regions and said doped depletion regions; said depletion regions have a net impurity concentration of the first conductivity type; said depletion regions has a net impurity concentration between 1E16 to 1E18 atom/cc..

33. The semiconductor device of claim 28 which further includes said doped depletion regions have a impurity concentration so that the built-in junction potential between said doped depletion regions and said substrate forms depletion regions in the substrate between the source/drain regions and the doped depletion region;

said depletion regions have a net impurity concentration of the first conductivity type.

34. The semiconductor device of claim 28 which further includes said doped depletion regions have a impurity concentration so that the built-in junction potential between said doped depletion regions and said substrate forms depletion regions in the substrate between the source/drain regions and the doped depletion region; said depletion regions have a net impurity concentration of the first conductivity type;

said depletion regions have a net impurity concentration between 1E16 to 1E18 atom/cc.

35. The semiconductor device of claim 28 which further includes one or more spacers on the sidewalls of said gate structure.